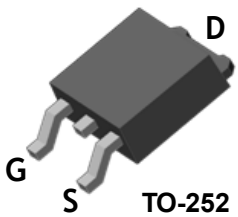
TSD840M
500V N-Channel MOSFET

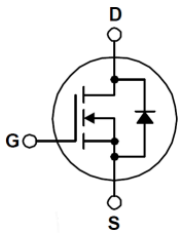
General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 9.0A,500V,Max.$R_{DS(on)}$=0.8 Ω @ V_{GS} =10V
- Low gate charge(typical 30nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability





Absolute Maximum Ratings

T_J=25℃ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		500	V
V_{GS}	Gate-Source Voltage		±30	V
I_D	Drain Current	T_C = 25℃	9.0*	A
		T_C = 100℃	5.4*	A
I_{DM}	Pulsed Drain Current	(Note 1)	36	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	303	mJ
E_{AR}	Repetitive Avalanche Energy	(Note 1)	6.3	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25℃)		130	W
	-Derate above 25℃		0.36	W/℃
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	℃

* Drain current limited by maximum junction temperature.

Thermal Resistance Characteristics

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	0.9	℃/W
$R_{\theta CS}$	Thermal Resistance,Case-to-Sink Typ.	--	℃/W
$R_{\theta JA}$	Thermal Resistance,Junction-to-Ambient	62.5	℃/W

Electrical Characteristics T_J=25 ℃ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.5 A	--	0.68	0.8	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	500	--	--	V
$\triangle BVDSS / \triangle TJ$	Breakdown Voltage Temperature Coefficient	ID = 250 uA, Referenced to 25℃	--	0.6	--	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 400 V, T_J = 125℃	--	--	10	uA
I_{GSSF}	Gate-Body Leakage Current,Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current,Reverse	V_{GS} =- 30 V, V_{DS} = 0 V	--	--	-100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1500	--	pF
C_{oss}	Output Capacitance		--	210	--	pF
C_{rss}	Reverse Transfer Capacitance		--	80	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS} = 250 V, I_D = 9.0A, R_G = 25 Ω (Note 4,5)	--	15	--	ns
t_r	Turn-On Rise Time		--	62	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	93	--	ns
t_f	Turn-Off Fall Time		--	48	--	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 9.0A, V_{GS} = 10 V (Note 4,5)	--	26	--	nC
Q_{gs}	Gate-Source Charge		--	4	--	nC
Q_{gd}	Gate-Drain Charge		--	13	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	9.0	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	24.0	A
V_{SD}	Source-Drain Diode Forward Voltage	I_S = 9.0 A, V_{GS} = 0 V	--	--	1.4	V
t_{rr}	Reverse Recovery Time	I_S =9.0A, V_{GS} = 0 V	--	348	--	ns
Q_{rr}	Reverse Recovery Charge	di_F/dt = 100 A/μs (Note 4)	--	3	--	uC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L=7.5mH, I_{AS}=9A, V_{DD}=50V, R_G=25 Ω,Starting TJ=25 ℃
3. I_{SD}≤9.0A, di/dt ≤ 200A/us, V_{DD} ≤ BV_{DSS}, Starting TJ = 25 ℃
4. Pulse Test: Pulse width ≤ 300us, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

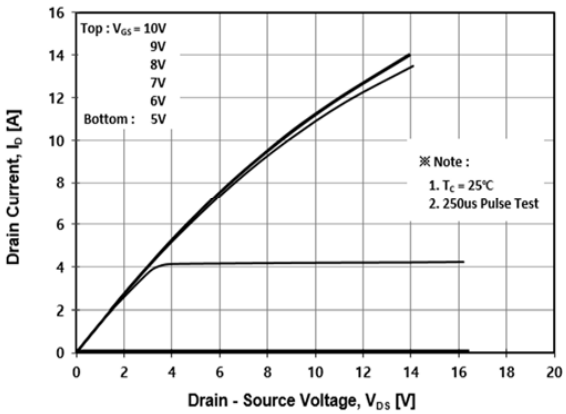


Fig. 2 Typical Output Characteristics

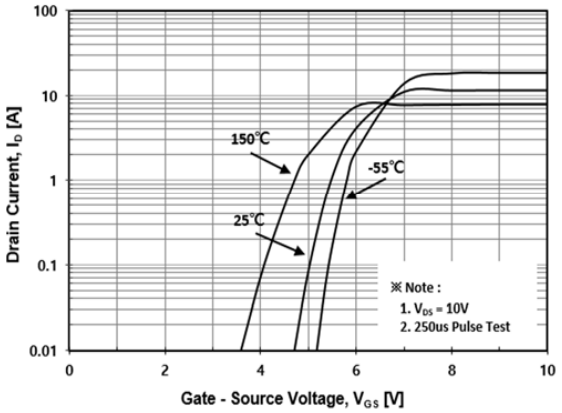


Fig.3 On-Resistance Variation with Drain Current and Gate

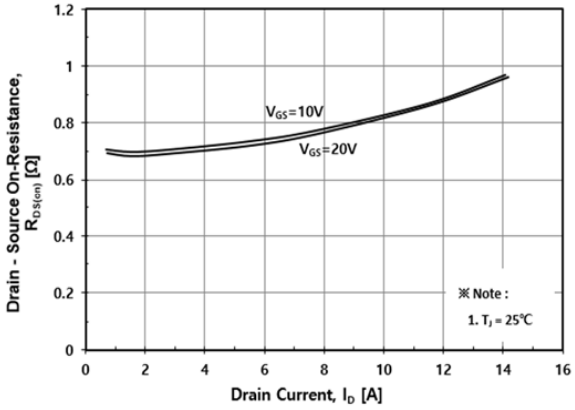


Fig. 4 Body Diode Forward Voltage Variation with Source Current and

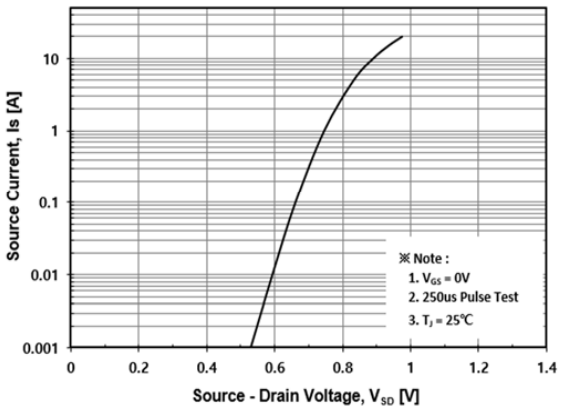


Fig. 5 Typical Capacitance Characteristics

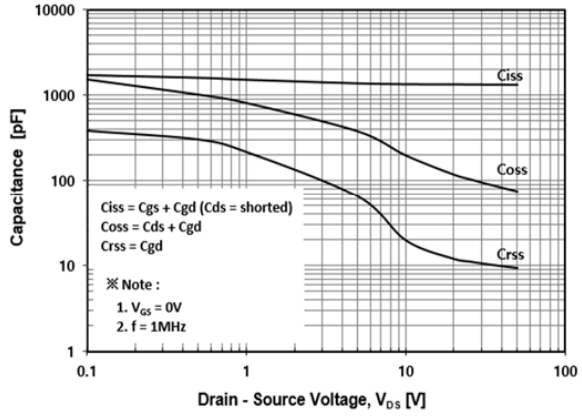


Fig. 6 Typical Total Gate Charge Characteristics

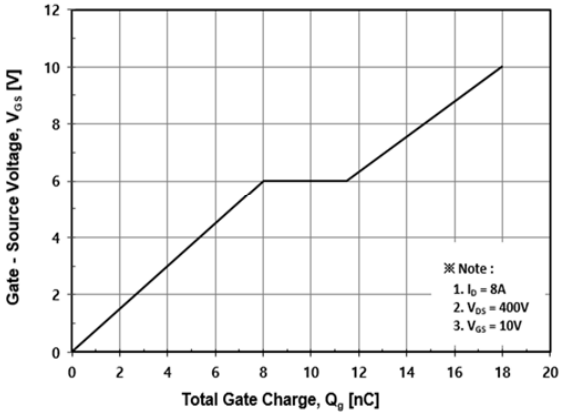


Fig. 7 Breakdown Voltage Variation vs. Temperature

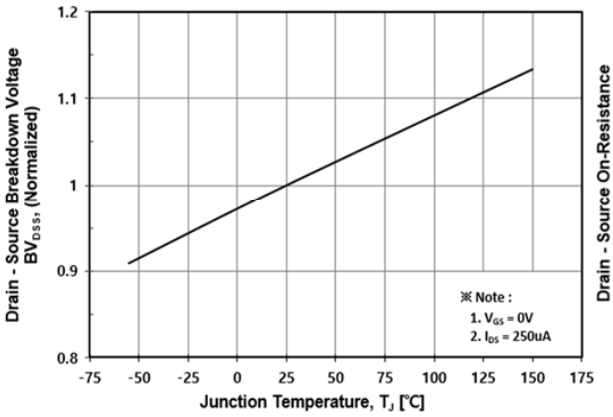


Fig. 8 On-Resistance Variation vs. Temperature

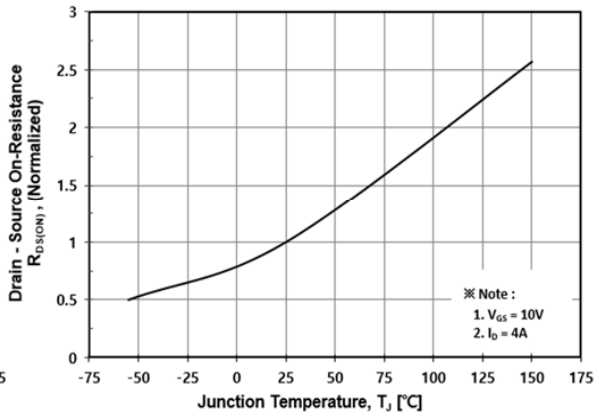


Fig. 9 Maximum Drain Current vs. Case Temperature

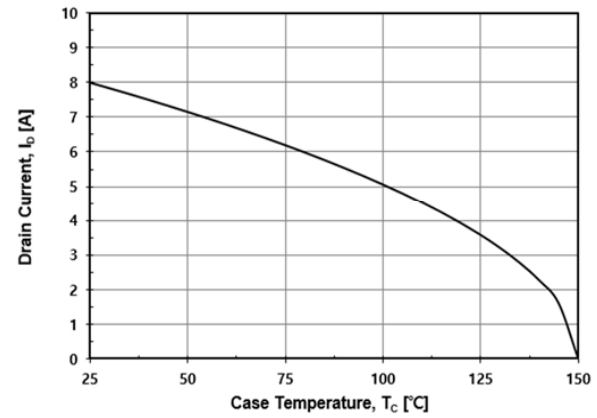


Fig. 10 Maximum Safe Operating Area

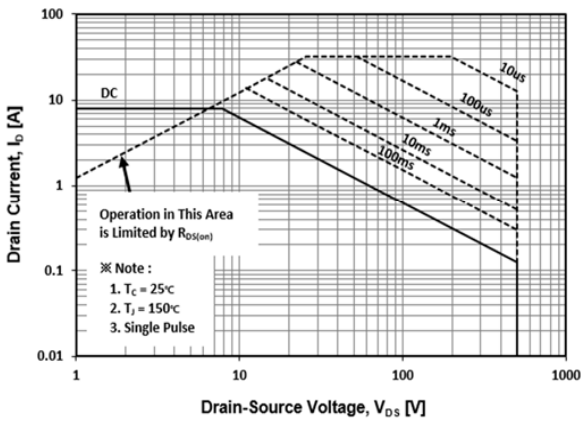


Fig. 11 Transient Thermal Impedance

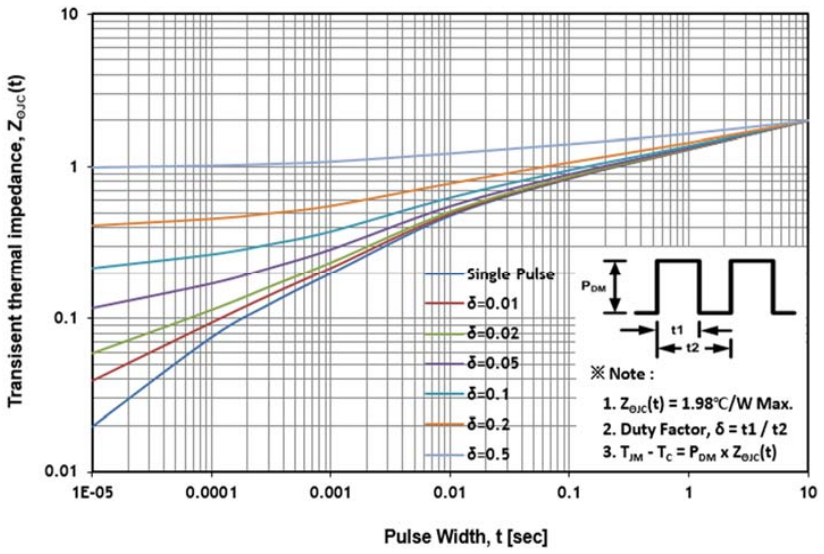
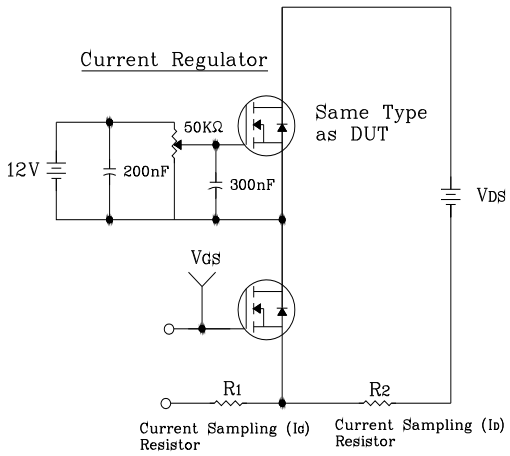


Fig. 12 Gate Charge Test Circuit & Waveform



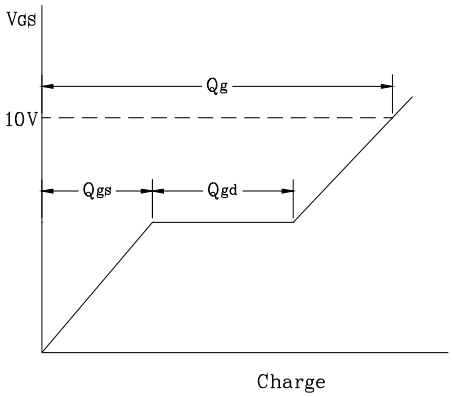
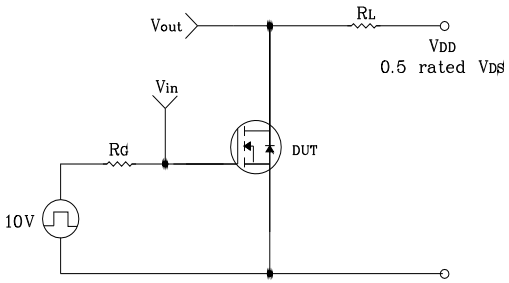


Fig. 13 Resistive Switching Test Circuit & Waveform



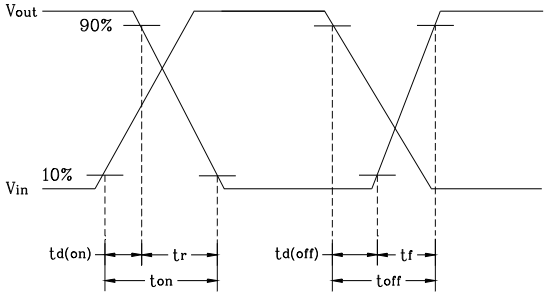
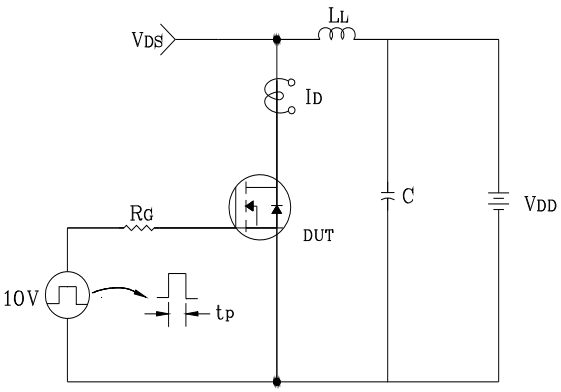


Fig. 14 E_{AS} Test Circuit & Waveform



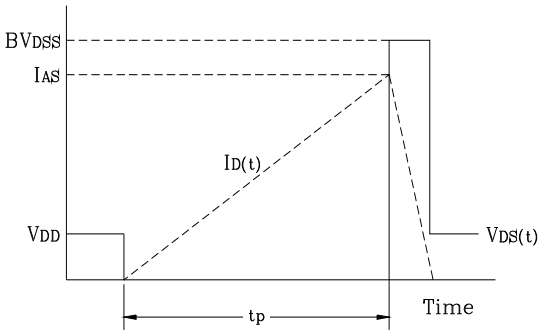


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform