

TSA20N65MR

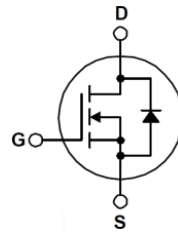
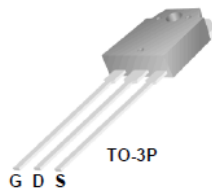
650V N-Channel MOSFET

General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 20A,650V, $R_{DS(on)}=0.48\Omega$ @ $V_{GS} =10V$
- Low gate charge(typical 57nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	± 30	V
I_D	Drain Current	$T_C = 25^\circ\text{C}$	20*
		$T_C = 100^\circ\text{C}$	12*
I_{DM}	Pulsed Drain Current	76*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	884	mJ
E_{AR}	Repetitive Avalanche Energy (Note 1)	10	mJ
I_{AR}	Repetitive avalanche current (Note 1)	20	A
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	192	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Resistance Characteristics

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.67	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	40	$^\circ\text{C/W}$

Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2	--	4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 10\ \text{A}$	--	0.40	0.48	Ω
g_{fs}	Forward transfer conductance(note 3)	$V_{DS} = 10\ \text{V}, I_D = 10\ \text{A}$ (Note 3)	--	40	--	S

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\ \text{V}, I_D = 250\ \mu\text{A}$	650	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650\ \text{V}, V_{GS} = 0\ \text{V}$	--	--	1	μA
		$V_{DS} = 650\ \text{V}, T_C = 125^\circ\text{C}$	--	--	100	
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	-100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1.0\ \text{MHz}$	--	4100	--	pF
C_{oss}	Output Capacitance		--	264	--	pF
C_{riss}	Reverse Transfer Capacitance		--	24	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 300\ \text{V}, I_D = 20\ \text{A},$ $R_G = 25\ \Omega$ (Note 3,4)	--	197	--	ns
t_r	Turn-On Rise Time		--	149	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	468	--	ns
t_f	Turn-Off Fall Time		--	83	--	ns
Q_g	Total Gate Charge	$V_{DS} = 480\ \text{V}, I_D = 20\ \text{A},$ $V_{GS} = 10\ \text{V}$ (Note 3,4)	--	57	65	nC
Q_{gs}	Gate-Source Charge		--	23	--	nC
Q_{gd}	Gate-Drain Charge		--	13	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I_S	Continuous Source-Drain Diode Forward Current	--	--	20	A	
I_{SM}	Pulsed Source-Drain Diode Forward Current	--	--	72		
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 20\ \text{A}, V_{GS} = 0\ \text{V}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$I_S = 20\ \text{A}, V_{GS} = 0\ \text{V}$ $di_F/dt = 100\ \text{A}/\mu\text{s}$ (Note 3,4)	--	435	--	ns
Q_{rr}	Reverse Recovery Charge		--	4.1	--	μC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=5\text{mH}, I_S=20\text{A}, V_{DD}=50\text{V}, R_G=25\Omega,$ Starting $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Typical Characteristics

Fig. 1 Typical Output Characteristics

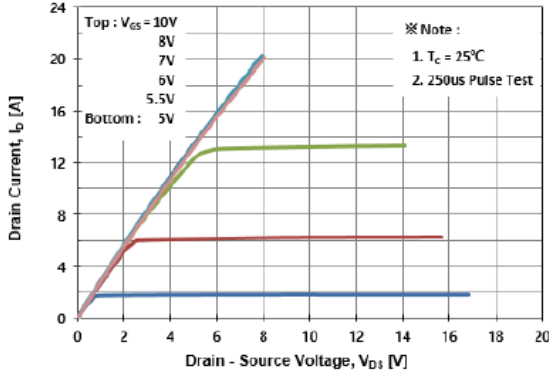


Fig. 2 Typical Output Characteristics

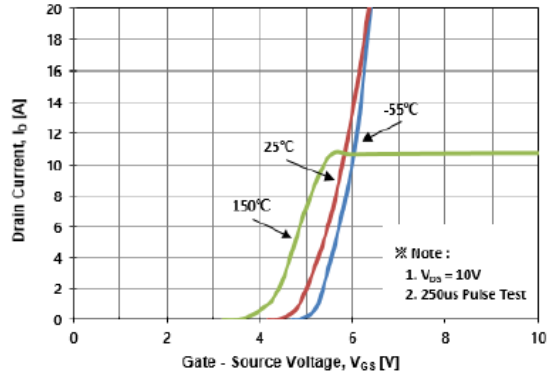


Fig. 3 On-Resistance Variation with Drain Current and Gate Voltage

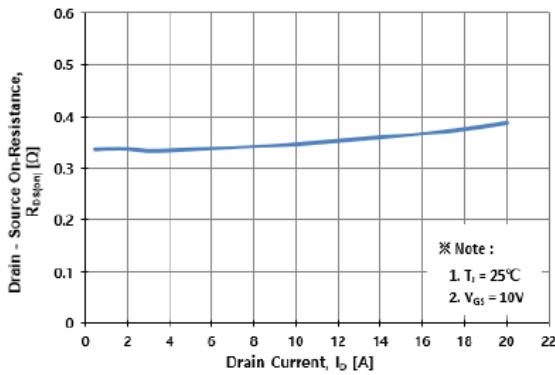


Fig. 4 Body Diode Forward Voltage Variation with Source Current

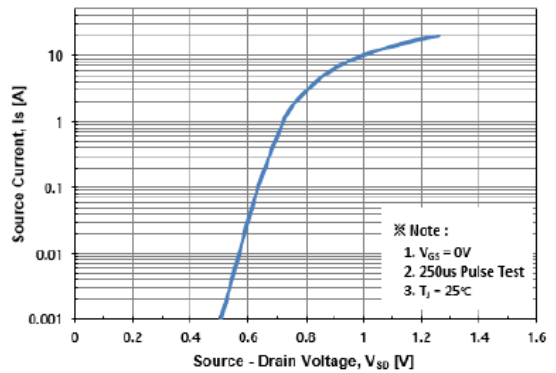


Fig. 5 Typical Capacitance Characteristics

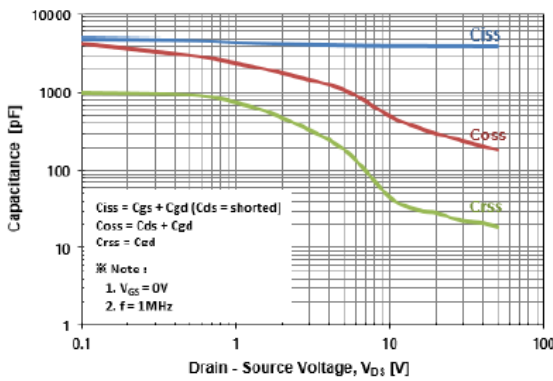
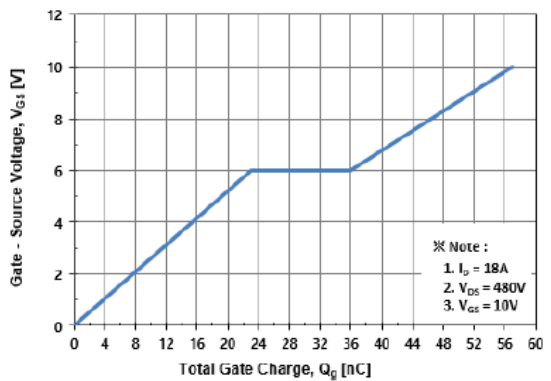


Fig. 6 Typical Total Gate Charge Characteristics



Typical Characteristics

Fig. 7 Breakdown Voltage Variation vs. Temperature

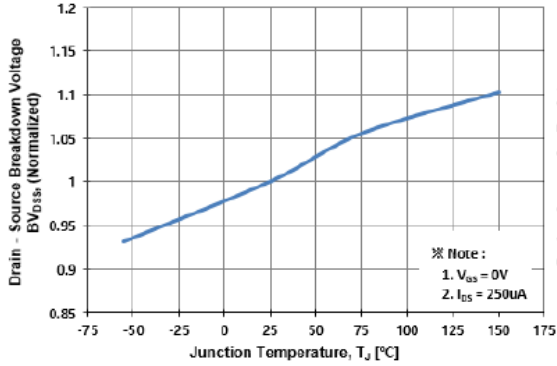


Fig. 8 On-Resistance Variation vs. Temperature

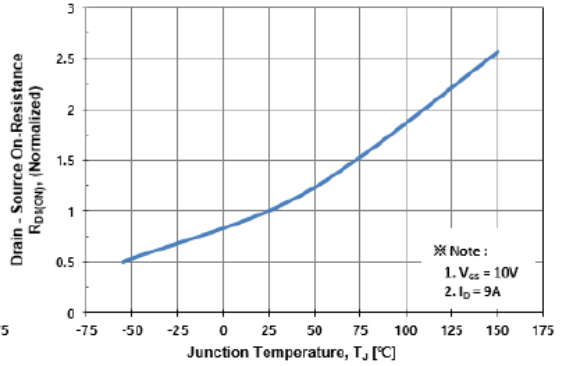


Fig. 9 Maximum Drain Current vs. Case Temperature

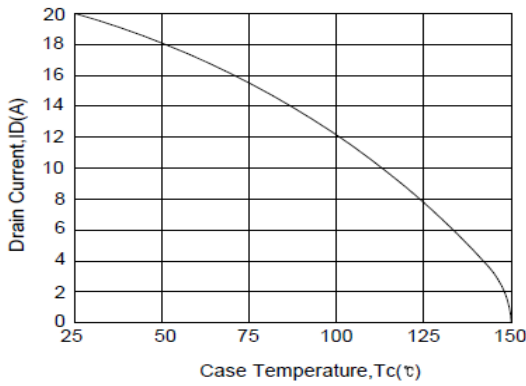


Fig. 10 Maximum Safe Operating Area

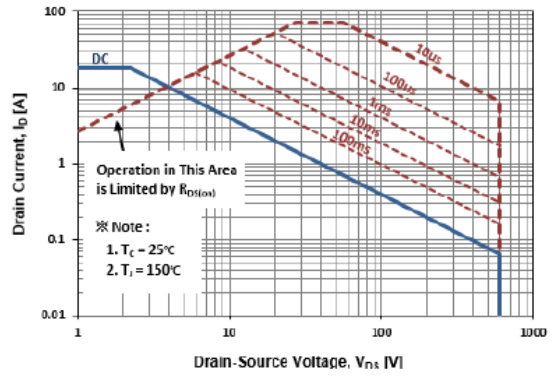


Fig. 11 Transient Thermal Impedance

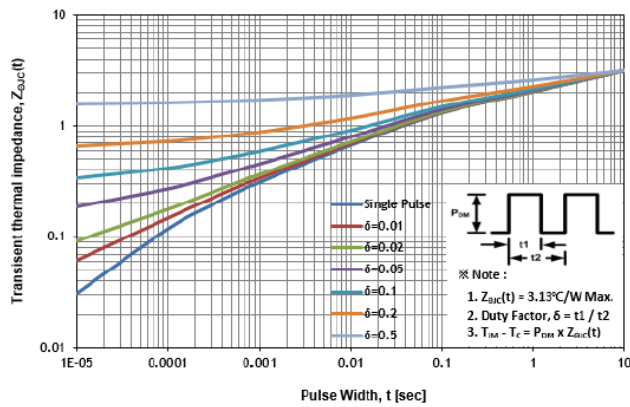


Fig 12. Gate Charge Test Circuit & Waveform



Fig 13. Resistive Switching Test Circuit & Waveforms

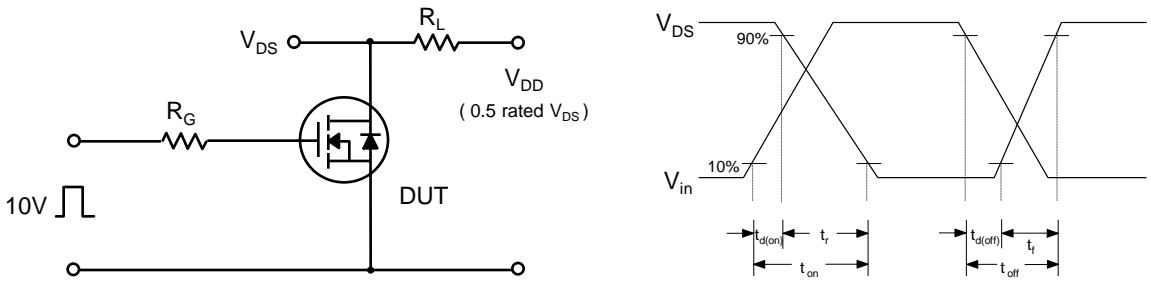


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

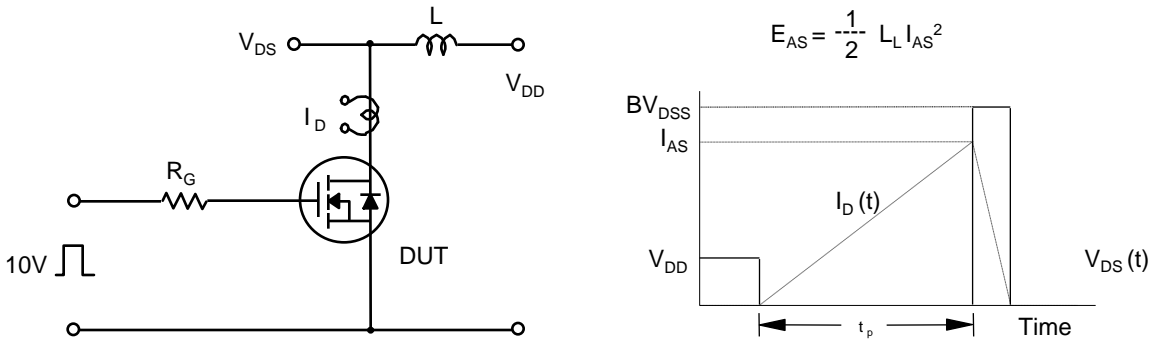


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

