Truesemi®

TSA65R190S3/TSK65R190S3

650V N-Channel MOSFET

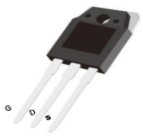
Description

SJ-FET is new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.
This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy.
SJ-FET is suitable for various AC/DC power conversion in switching mode operation for higher efficiency.

Features

- 20A,650V,Max.RDS(on)=0.19Ω @ VGS =10V
- Low Power Loss by High Speed Switching and Low On-Resistance
- ③ 100% Avalanche Tested

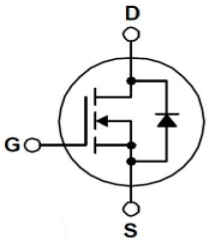
TSA65R190S3



TO-3P

TSK65R190S3

TO-247



Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter		TSA65R190S3	TSK65R190S3	Units
V_{DSS}	Drain-Source Voltage		650		V
V_{GS}	Gate-Source Voltage		± 30		V
I_D	Drain Current	T_C = 25℃	20		A
		T_C = 100℃	14		A
I_{DM}	Pulsed Drain Current	(Note 1)	60		A
E_{AS}	Single Pulsed Avalanche Energy		485		mJ
P_D	Power Dissipation (T_C = 25℃)		258	265	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		℃

Thermal Resistance Characteristics

Symbol	Parameter	TSA65R190S3	TSK65R190S3	Units
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	0.47	0.47	℃/W
$R_{\theta JA}$	Thermal Resistance,Junction-to-Ambient	65	65	℃/W

Electrical Characteristics T_C=25 ℃ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.5 A	--	0.17	0.19	Ω
g_{fs}	Forward transfer conductance	V_{DS} = 15V, I_D = 4.5A (Note 4)	--	12	--	S
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	650	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 650 V, T_C = 125℃	--	--	100	uA
I_{GSSF}	Gate-Body Leakage Current,Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current,Reverse	V_{GS} =- 30 V, V_{DS} = 0 V	--	--	-100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1805	--	pF
C_{oss}	Output Capacitance		--	1400	--	pF
C_{rss}	Reverse Transfer Capacitance		--	70	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{GS} = 10V, R_G = 25Ω, V_{DS} = 350V, I_D = 20 A	--	40	--	ns
t_r	Turn-On Rise Time		--	75	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	172	--	ns
t_f	Turn-Off Fall Time		--	75	--	ns
Q_g	Total Gate Charge	V_{GS} = 10V, V_{DS} =560V, I_D = 20 A	--	53	68	nC
Q_{gs}	Gate-Source Charge		--	13	--	nC
Q_{gd}	Gate-Drain Charge		--	20	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	20	A
V_{SD}	Source-Drain Diode Forward Voltage	I_S = 20A, V_{GS} = 0 V	--	--	1.4	V
t_{rr}	Reverse Recovery Time	I_S = 20A, V_{GS} = 0 V, di_F/dt = 100 A/μs	--	524	--	ns
Q_{rr}	Reverse Recovery Charge		--	9.4	--	uC
Irrm	Reverse Recovery Current		--	35.7	--	A

NOTES:

1. Pulse width t_P limited by $T_{j,max}$

2.$I_{SD} \le I_D$, $V_{DS\ peak} \le V_{(BR)DSS}$

3. $C_{o(er)}$ is a capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0V to 80%

■ Characteristic Graph

Fig.1 On-Region Characteristics.

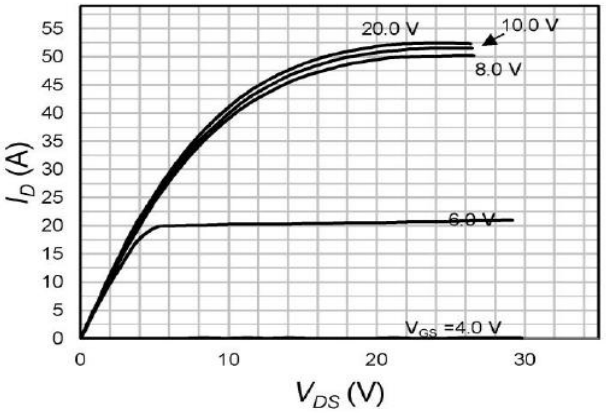


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

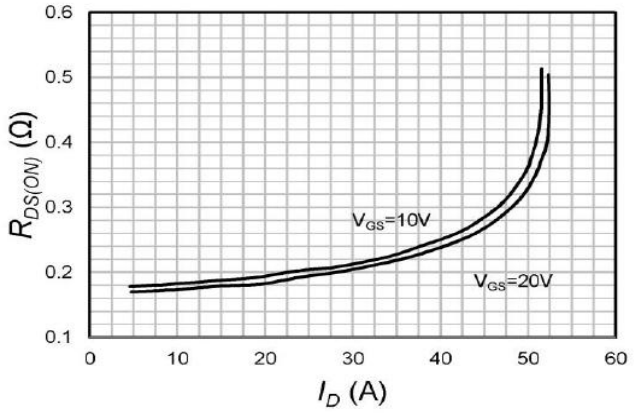


Fig.3 On-Resistance Variation with Temprature (Normalized)

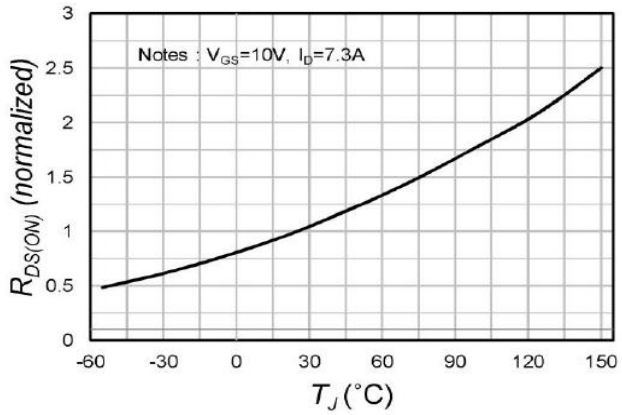


Fig.4 Breakdown Voltage Variation vs. Temperature (Normalized)

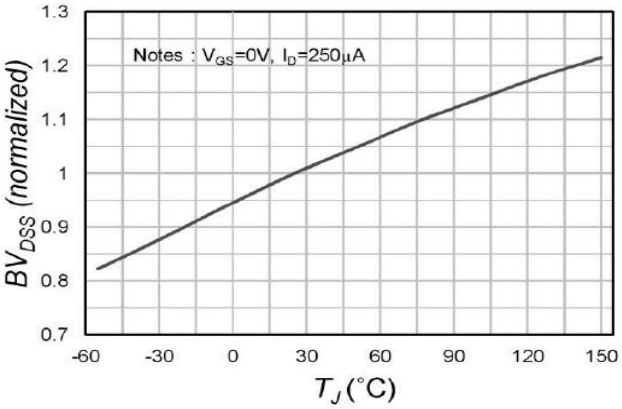


Fig.5 Transfer Characteristics

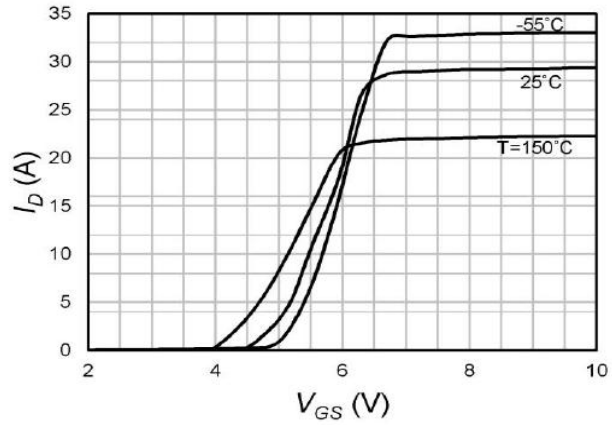


Fig.6 Body Diode Forward Voltage Variation with Source Current and Temperature

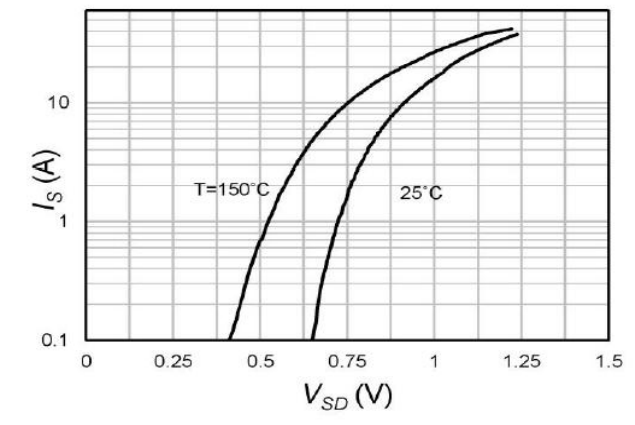


Fig.7 Gate Charge Characteristics

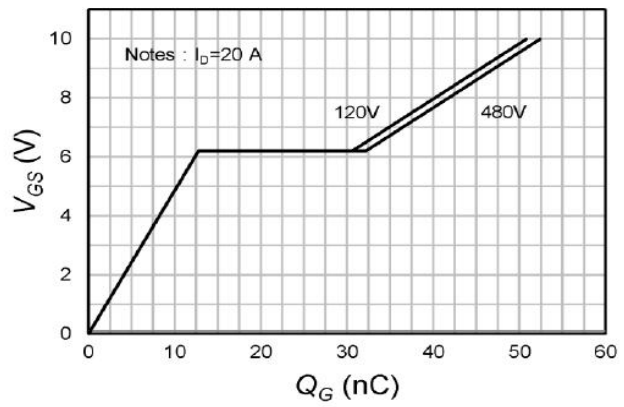


Fig.8 Capacitance Characteristics

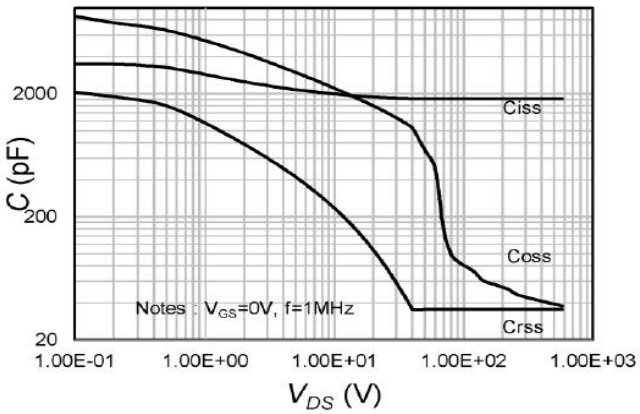


Fig.9 $V_{GS(th)}$ Variation with Temprature (Nomalized)

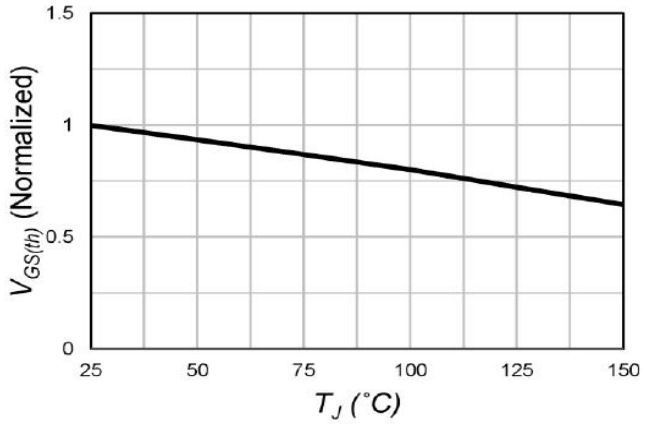


Fig.10 Maximum Drain Current vs. Case Temperature

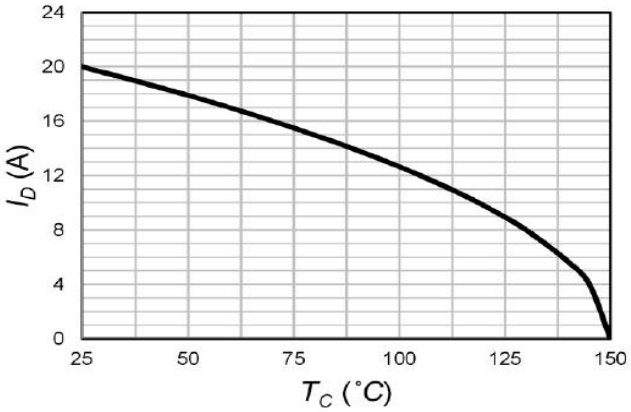


Fig.11 Single Pulse Maximum Power Dissipation

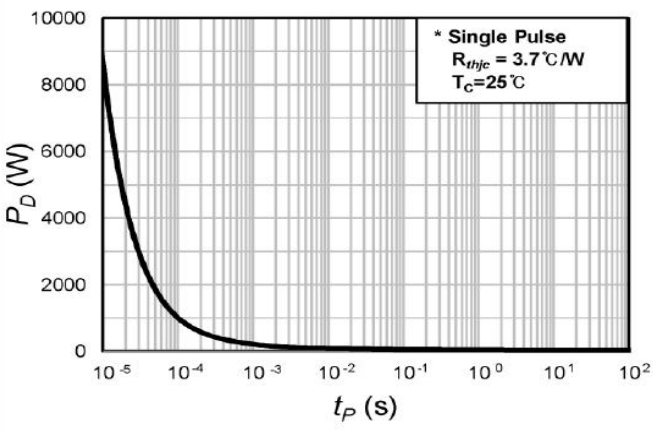


Fig.12 Output Capacitance Stored Energy

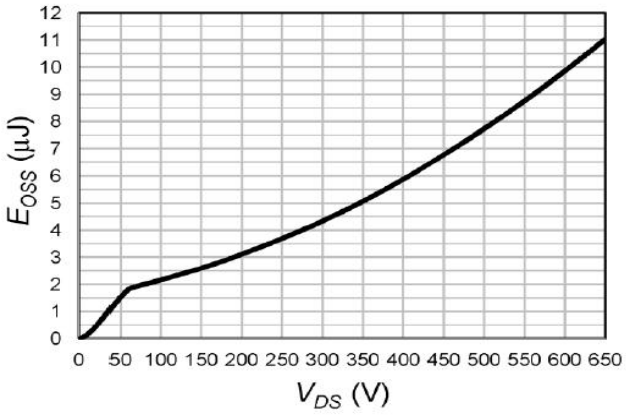


Fig.13 Transient Thermal Response Curve

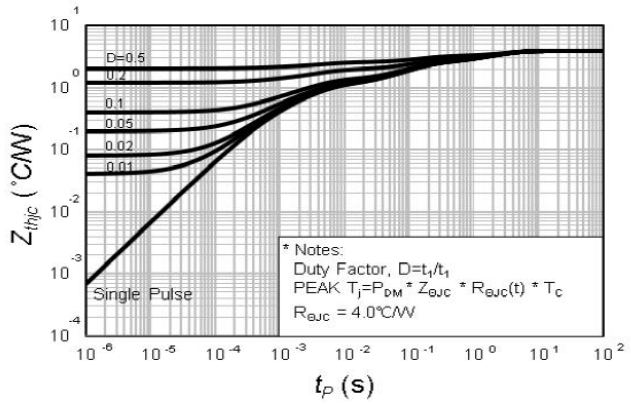
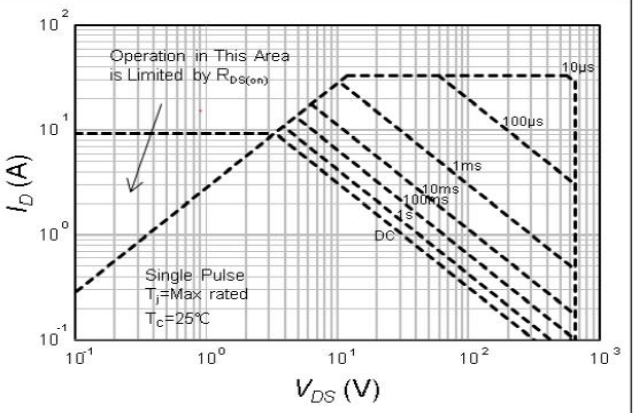


Fig.14 Maximum Safe Operating Area



■ Test Circuit

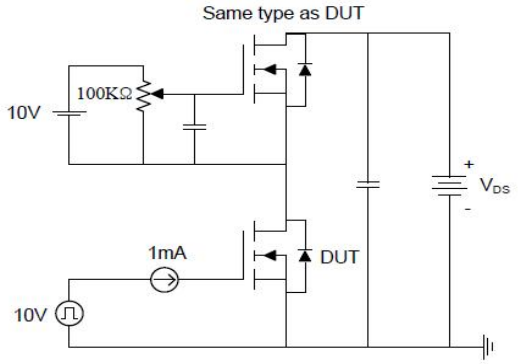


Fig15-1. Gate charge measurement circuit

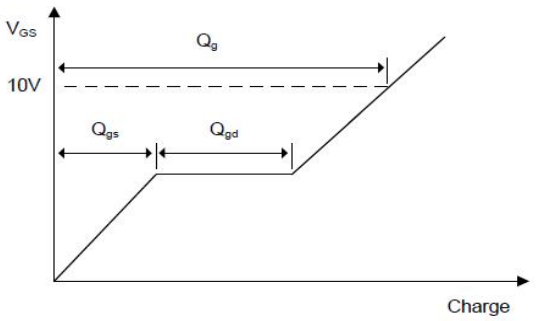


Fig15-2. Gate charge waveform

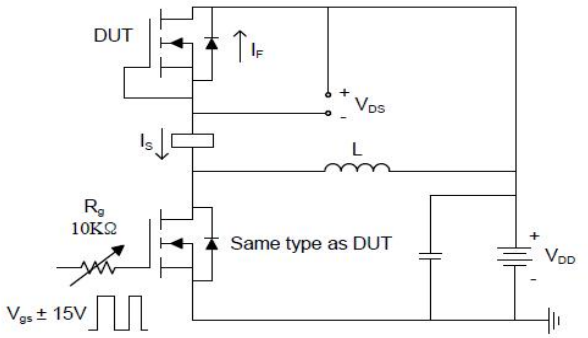


Fig16-1. Diode reverse recovery test circuit

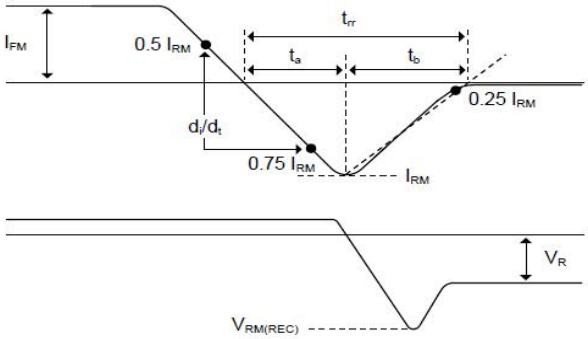


Fig16-1. Diode reverse recovery test waveform

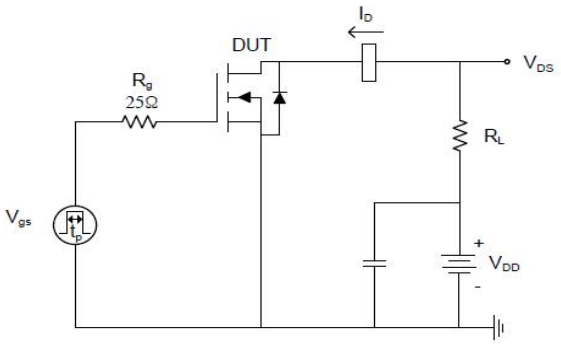


Fig17-1. Switching time test circuit for resistive load

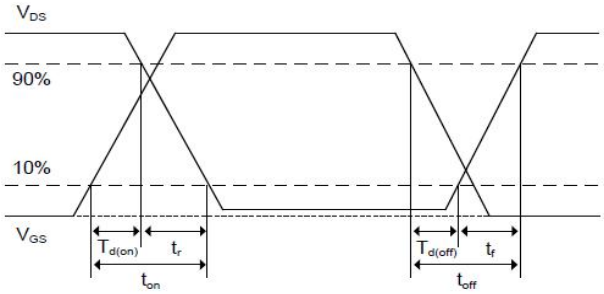


Fig17-2. Switching time waveform

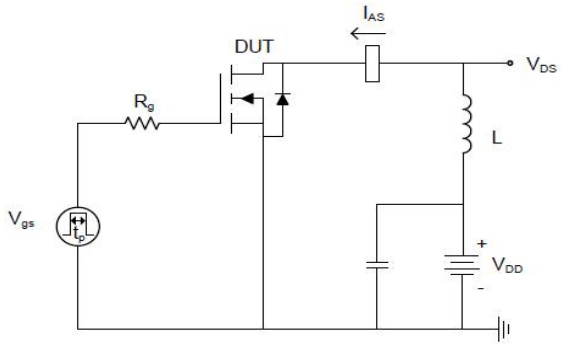


Fig18-1. Unclamped inductive load test circuit

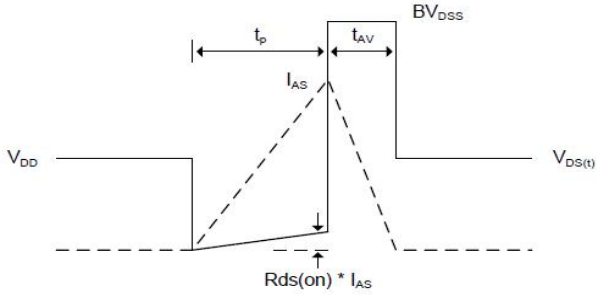


Fig18-2. Unclamped inductive waveform